14.7 An Integrated Draft 802.11n Compliant MIMO Baseband and MAC Processor

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The wireless LAN industry has undergone explosive growth in recent years. Transmission speeds have been increasing leaps and bounds with each generation of WLAN product. 802.11b delivered 11Mb/s and 802.11g followed with a 5-fold increase taking the speeds to 54Mb/s. The industry has been working on the new 802.11n standard to deliver an unprecedented speed of 600Mb/s, an 11-fold increase in transmission speed over 802.11g, using MIMO technology. A MIMO-based 802.11n draft compliant [1] chip is presented that employs 3 transmit and 3 receive antennas to improve the robustness of MIMO transmission. This integrated baseband (BB) and MAC chip supports up to 2 spatial streams and hence can deliver 300Mb/s of transmission speed in 40MHz bandwidth and 135Mb/s in 20MHz bandwidth. The MIMO physical layer in conjunction with the 802.11n MAC can deliver a user throughput (TCP) in excess of 150Mb/s. Also this 802.11n solution achieves a range close to 700ft.

The system overview is shown in Fig. 14.7.1. This MIMO system has a radio chip that has 3 transmit and 3 receive chains, which down-converts the received signals and up-converts the transmitted signals and also performs filtering operations. The radio chip interfaces with the MAC/BB chip. On the receive side, the signals from the multiple antennas are fed into the BB receive processing logic, where the MIMO streams are decoded and the information bits are passed onto the Protocol Control Unit (PCU). On the transmit side, the information bits are coded into multiple streams and fed into the multiple radio chains for transmission. PCU manages all low-level, timing critical aspects of 802.11. It formats and sends outgoing frame data to the BB transmitter and processes incoming frame data from the BB receiver. The DMA engine manages transfer of frame data and control information between the PCU and the host interface unit (HIU). The HIU provides connectivity to the host over a PCI/PCIe bus.

Figure 14.7.2 is a detailed block diagram of PCU and BB. The figure shows the 3 transmitter and 3 receiver BB logic and the various MAC/PCU blocks related to the new aggregation scheme in 802.11n.

The BB transmitter has 3 transmitter chains and operates in 1, 2, or 3-chain mode. The transmitter can support up to 2 spatial streams. The transmitter generates High Throughput (HT) waveforms according to the draft 802.11n specifications and legacy waveforms according to the 802.11a/g specifications. The 802.11n specification supports a mode, called dynamic 20/40 mode, where the transmitter can decide to dynamically switch between 20MHz and 40MHz transmission, based on the activity of the channel, and the receiver should detect this switch and receive the signals properly. In this mode, a 256-point IFFT is used to generate HT40 packets, and a 128-point IFFT is used to generate HT20 and legacy OFDM packets. HT20 and legacy OFDM/CCK packets are generated centered at DC, then frequency shifted digitally to the control channel. Per stream cyclic shift diversity (CSD) and spatial spreading is applied before IFFT, and per chain CSD is applied after IFFT. Dual 9b 160/176MHz DACs pass BB data to the analog transceiver in each chain.

The BB receiver has 3 receiver chains and can operate in 1, 2, or 3-chain mode. Each chain contains dual 9b 80/88MHz ADCs that cover ±500mV input range. The AGC in each chain performs independent but synchronized gain changes to size the signal to a target level at the ADC input (see Fig. 14.7.2). The receiver gain is composed of RF, IF, and BB gains, as well as an antenna switch that provides additional attenuation. The AGC sized signal after timing, DC and frequency compensation is combined across multiple chains using a MIMO equalizer and its output is de-interleaved and decoded.

The receiver operates in dynamic 20/40 mode by default. Figure 14.7.3 shows the details inside the AGC/DC offset/Timing Offset/Frequency Offset block in Fig. 14.7.2. After DC offset removal, the ADC outputs are frequency shifted by ±10MHz, low pass filtered and down-sampled to generate two signals, one for each 20MHz sub-channel. Signal detection is performed in each sub-channel to identify 20/40MHz and OFDM/CCK. The signal of the right bandwidth is chosen and processed in the right data path based on the packet type. A 256-point FFT is used in the dynamic 20/40MHz mode, and a 128-point FFT is used for static 20MHz mode. The receiver can also operate in static mode as a legacy 802.11a/g device.

The receiver performs frequency offset estimation, symbol timing estimation, and channel estimation using the preamble. It dynamically detects an HT packet format, and performs HT channel estimation for HT packets. The receiver supports up to 2 spatial streams. Continuous pilot track is performed to correct residual frequency offset errors and phase noise. Minimum Mean Square Error (MMSE) MIMO equalizer coefficients [2] are computed from the HT channel estimation. The equalized data is passed to a radix-4, fully parallel, traceback architecture Viterbi decoder, which implements bin weighting based on the reliability of the equalized data. Short GI mode is supported.

Figure 14.7.4 shows the SNR required by the implementation in a cabled diagonal channel for 2 streams, HT40, 2×2 and 3×3, at 10% packet error rate.

The MAC is responsible for many tasks which are timing critical in the 802.11 specification, while software is responsible for queuing transmit packets and de-queuing receive packets using a descriptor chain mechanism. In addition to the logic to support the standard features of 802.11, new features have been added to support the high performance needs of 802.11n. Higher data rates offered by 802.11n will result in worse than the existing 802.11a/g MAC efficiencies and hence the need for an improved MAC. The 802.11n frames have a legacy Physical Layer Convergence Protocol (PLCP) and a HT PLCP. For example, a 1540 byte packet transmitted at the fastest rate for legacy OFDM (54Mb/s) will take 232µs to transfer the payload on the air. This same packet will take only 44µs when 300Mb/s HT rate is used. Accounting for the extra time to send the PLCP and the ACK time and the average random back-off, it is worth noting that the legacy packets are transmitted with 54% efficiency. However the HT packets will be transmitted with only 16% efficiency. To improve MAC efficiency, 802.11n uses aggregation of multiple MAC frames to form a signal PHY level frame. This can improve the efficiency to 82% for a 32-packet aggregation. Aggregation relies on the MAC treating each packet within an aggregate as a separate packet with it's own FCS so that if individual packets fail in an aggregate the entire aggregate does not need to be re-transmitted but rather just the packets which failed FCS. Normally a response ACK is used to let the transmitter know whether the receiver received a packet successfully. For aggregates, the receiver transmits a block ACK that holds a bitmap to acknowledge up to 64 unique packets based on their sequence numbers. The MAC is responsible for packing the individual packets data and associated descriptor in the transmit FIFO and forming an aggregate that is composed of packets separated by delimiters. If a corrupted delimiter is detected on receive, the MAC will continue to scan the data stream for a delimiter and assumes that packet data will follow.

The MAC maintains a 16 entry cache of block ACK bitmaps for recent packets. Each entry is associated with a MAC address and a QoS traffic identifier (TID). If an aggregate is received and the transmitter address matches the MAC address and the TID also matches then the bitmap will be updated with the successful packets of the aggregate.

The technology, dimension and power consumption of the chip are presented in Fig. 14.7.5. The die micrograph is shown in Fig. 14.7.6. Figure 14.7.7 is a plot of the user TCP throughput as a function of distance. The reported measurements are average numbers across 4 different orientations. These measurements were performed in an environment which has a mix of LOS and non-LOS locations. The AP uses standard dual-band dipole antennas, while the station uses a cardbus card with printed antennas. At close end, >150Mb/s is achieved and the range extends up to 700ft.

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References:

[1] Draft 802.11n Standard, IEEE P802.11n/D1.0, March, 2006.
[2] A. Paulraj, and C. Papadias, "Space-time Processing for Wireless Communications," *IEEE Signal Processing Magazine*, pp. 49-83, Nov., 1997.

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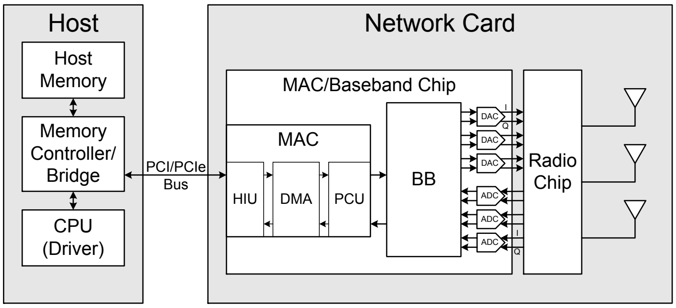

Figure 14.7.1: System Overview.

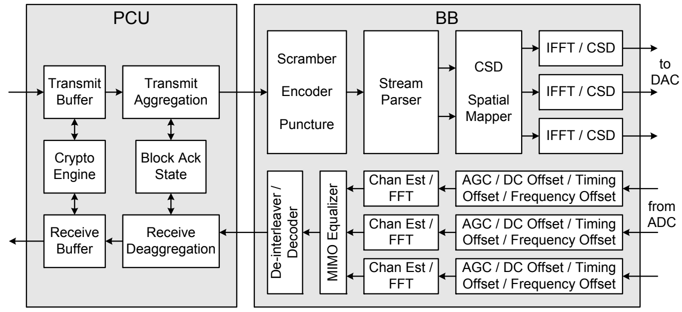

Figure 14.7.2: MAC(PCU)/BB Detailed Architecture (All interfaces within PCU are 32 bits. PCU-BB interface is 8b wide. ADC output and DAC input are 9b wide, all other interfaces in the BB are 12b wide).

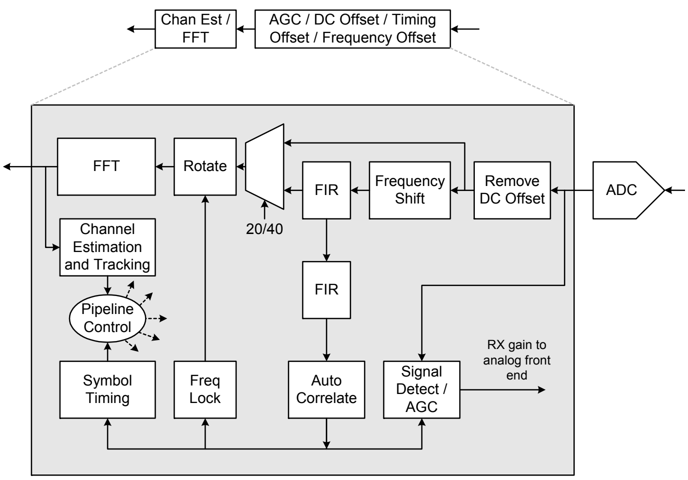

Figure 14.7.3: Block diagram of AGC/DC-Offset/Timing-Offset/Frequency-Offset and channel estimation. (ADC output is 9b wide, all other interfaces are 12b wide.)

MCS	Modulation	Coding Rate	Data rate (Mbps)	Required SNR (dB) 2x2	Required SNR (dB) 3x3
8	BPSK	½	27	3.1	2.0
9	QPSK	½	54	6.4	4.6
10	QPSK	2/3	72	8.9	7.4
11	16QAM	½	108	12.3	10.5
12	16QAM	2/3	144	15.9	14.2
13	64QAM	½	216	20.2	18.3
14	64QAM	¾	243	21.7	19.6
15	64QAM	5/6	300	23.5	21.4

Figure 14.7.4: SNR required by the chip to maintain 10% PER for 2 streams, HT40 in a diagonal cabled channel.

Technology	0.18um, CMOS, 6 layer metal
Core voltage	1.8V, IO voltage: 3.3V
Die dimension	7840 x 7760um (scribe not included scribe is 80um wide)
Chip dimension	14 x 14 mm
Package	304 pin BGA
Transistor count	14.24 M
Power (Rx/Tx)	
• Core	972 / 630 mW
• ADC/DAC	277 / 277 mW
• MISC	25 / 25 mW
• I/O	105 / 178 mW
• Total Power	1379 / 1110 mW

Figure 14.7.5: Chip Details.

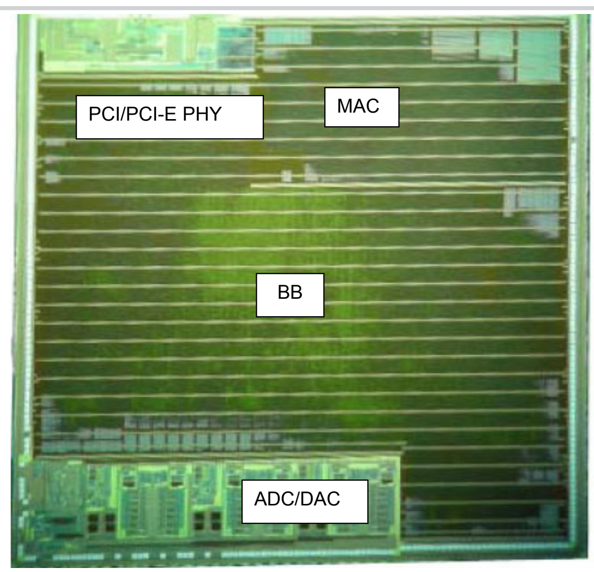

Figure 14.7.6: Die micrograph.

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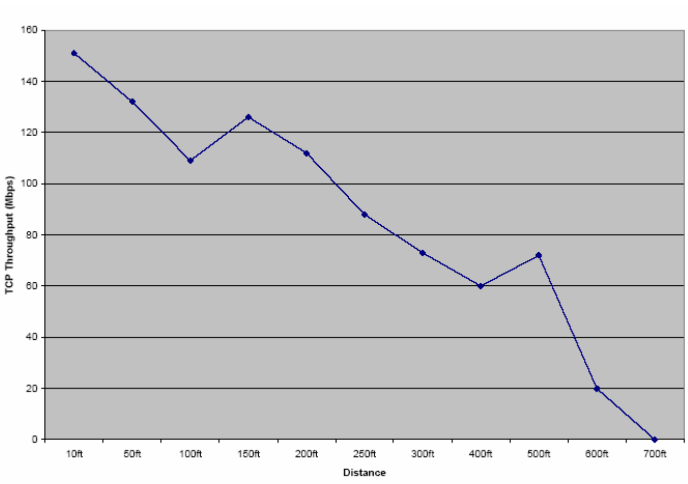

Figure 14.7.7: TCP Throughput over range performance curve.

